REMARKS

Claims 1-24 were pending in this patent application. Claims 1 and 2-15 have been amended and no new matter has been added. Claim 23 has been cancelled. Accordingly, claims 1-22 and 24 remain pending in the present patent application. Applicants respectfully submit that the pending claims are now in condition for allowance. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

Present Invention

A method for testing a high-speed circuit is disclosed. The high-speed circuit has a first frequency of greater than one GHz and the high-speed circuit being a high-speed phase and clock recovery circuit. The method comprises obtaining a high-speed statistical signature of the high-speed circuit by oversampling an output of the high-speed circuit using a tester having a second frequency of not greater than one GHz. The tester is external to the high-speed circuit. The method further comprises comparing the high-speed statistical signature of the high-speed circuit to an expected signature.

Rejections – 35 U.S.C. 103(a)

The Examiner states,

6. Claims 1, 15, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829B1) in view of Ooishi (US 6,396,768B2) and Talley (US 5,301,156). As per claim 1, Schneider teaches a method for testing a high-speed circuit having a first frequency of greater than one GHz (fig. 5, col. 9, lines 8-11, col. 11, lines 17-50, Schneider), the high-speed circuit being a high-speed phase and clock recovery circuit (fig. 5, col. 7, lines 9-12, Schneider). However Schneider does not explicitly teach the specific use of obtaining a high-speed statistical signature of the high-speed circuit using a tester; comparing the high-speed statistical signature of the high-speed circuit to an expected signature.

Talley in an analogous art teaches that signature generator 412 ... data errors have occurred (col. 7, lines 34-52, Talley).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Talley by including an additional step of obtaining a high-speed statistical signature of the high-speed circuit using a tester; comparing the high-speed statistical signature of the high-speed circuit to an expected signature. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to produce a signature, which is statistically related to the correctness of a stream of data and verify the correct operation of the high-speed circuit.

Schneider also does not explicitly teach using a tester having a second frequency of not greater than one GHz, the tester being external to the high-speed circuit.
However Ooishi in an analogous art teaches easy detection of a failure by the tester even if the tester applies external clock signal ext.ClK of a low frequency to the SDRAM, and therefore the SDRAM can be tested by a more inexpensive tester (fig. 3, 52, 65, abstract, col. 42, lines 12-15, Ooishi).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Ooishi by including an additional step of using a tester having a second frequency of not greater than one GHz, the tester being external to the high-speed circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce cost of testing a high-speed circuit.

- **As per claim 15, Schneider, Ooishi and Talley teach the additional limitations.**

Schneider teaches a system for testing a high-speed circuit having a first frequency of greater than one GHz, the high-speed circuit being a high-speed phase and clock recovery circuit, the system comprising: at least one computer system, coupled with the tester (Fig. 5, col. 7, lines 9-1, col. 8, lines 32-42, col. 9, lines 8-11, col. 11, lines 17-50, Schneider).

Talley teaches obtaining a high-speed statistical signature of the high-speed circuit using the tester and for comparing the high-speed statistical signature of the high-speed circuit to an expected signature (col. 7, lines 34-52, Talley).

Ooishi teaches a tester for providing at least one signal to the high-speed circuit, the tester having a second frequency of not greater than one GHz, the tester being external to the high-speed circuit (fig. 3, 52,65, abstract, col. 42, lines 12-15, Ooishi).

- **As per claim 23, Schneider, Ooishi and Talley teach the additional limitations.**

Schneider teaches the system further comprising means for repeating the utilizing, reading, providing and repeating steps a particular number of times (col. 8, line 21-col. 9, line 11, Schneider).

7. Claims 2, 3, 4, 5, 6, 7, 8, 9, 16, 17, 18, 19, 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829B1), Ooishi (US 6,396,768B2) and Talley (US 5,301,156) as applied to claim 1, 15 above, and further in view of Wong et al. (US 5,329,559). As per claim 2, Schneider, Ooishi and Talley substantially teach the claimed invention described in claim 1 (as rejected above). Schneider also teaches utilizing the tester to provide a signal to the high-speed phase and clock recovery circuit, and reading an output signal from the high-speed phase and clock recovery circuit; repeating the utilizing and reading steps a particular number of times (fig. 5, col. 7, lines 9-12, col. 8, line 21 to col.

9, line 11, Schneider). However Schneider and Talley do not explicitly teach the specific use of the signal having a delay corresponding to a phase change.

Wong et al. in an analogous art teaches phase error between the incoming data signal and the PLL clock signal (abstract, Wong et al.). Wong et al. also teach that data signals in the data recovery signal path must be delayed by the same amount of time as the signals, which go through the non-linear element used for clock recovery (col. 1, lines 60-63, Wong et al.). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Wong et al. by including an additional step of using the signal having a delay corresponding to a phase change.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the signal having a delay corresponding to a phase change would provide the opportunity to time synchronize the test signal transition and the clock signal.

- **As per claim 3, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches performing the utilizing, reading and repeating steps (fig. 5, col. 7, lines 9-12, col. 8, line 21 to col. 9, line 11, Schneider). Wong et al. teach a second delay (col. 9, lines 64-67, Wong et al.).**
- **As per claim 4, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Talley teaches the method wherein the utilizing step further includes the step of: setting the delay using the tester (col. 29, lines 41-49, Talley).**
- **As per claim 5, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Wong et al. teach the method wherein the high-speed phase and clock recovery circuit includes an internal data recovery phase setting, and wherein the utilizing step further includes the step of: determining the delay using the internal data recovery phase setting (col. 1, lines 60-63, col. 2, lines 62-63, Wong et al.).**
- **As per claim 6, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches the method wherein the high-speed phase and clock recovery circuit further includes at least one latch and wherein the output signal reading step further includes the step of: reading sampled data from at least one oversampled latch (col. 7, line 49 to col. 8, line 1, Schneider).**
- **As per claim 7, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Talley teaches a parallel bus and wherein the output signal reading step further includes the step of: reading sampled data from the parallel bus (fig. 4, 7, col. 5, lines 67-68, col. 7, lines 53-68, Talley).**
- **As per claim 8, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches the method wherein the high-speed circuit is a high-speed phase and clock recovery circuit, utilizing the tester to provide a signal to the high-speed phase and clock recovery circuit, reading an output signal from the high-speed phase and clock recovery circuit; and repeating the utilizing and reading steps (fig. 5, col. 7, lines 9-12, col. 8, line 21 to col. 9, line 11, Schneider). Wong et al. teach the signal having a delay corresponding to a phase change (abstract, col. 1, lines 60-63, Wong et al.) and providing at least one new delay (col. 9, lines 64-67, Wong et al.).**
- **As per claim 9, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches the method further comprising the steps of: repeating the utilizing, reading, providing and repeating steps a particular number of times (fig. 5, col. 8, line 21 to col. 9, line 11, Schneider).**
- **As per claim 16, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations.**

Schneider teaches the system, wherein the tester further reads at least one output signal from the high speed phase and clock recovery circuit a particular number of times to provide statistical data for the high-speed statistical signature (fig. 5, col. 7, lines 9-12, col. 8, line 21 to col. 9, line 11, Schneider). Wong et al. teach that the at least one signal has a delay corresponding to a phase change (abstract, col. 1, lines 60-63, Wong et al.).

- **As per claim 17, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches the system wherein the tester further provides the at least one signal, reads the at least one output signal the particular number of times (fig. 5, col. 8, line 21 to col. 9, line 11, Schneider). Wong et al. teach a second delay (col. 9, lines 64-67, Wong et al.).**
- **As per claim 18, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Talley teaches the system wherein the tester further sets the delay (col. 29, lines 41-49, Talley).**
- **As per claim 19, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Wong et al. teach the system wherein the high-speed phase and clock recovery circuit includes an internal data recovery phase setting that is used to set the delay (col. 1, lines 60-63, col. 2, lines 62-63, Wong et al.).**
- **As per claim 20, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Schneider teaches the system wherein the high-speed phase and clock recovery circuit further includes at least one latch and wherein the tester further receives sampled data from at least one oversampled latch (col. 7, line 49 to col. 8, line 1, Schneider).**
- **As per claim 21, Schneider, Ooishi, Talley and Wong et al. teach the additional limitations. Talley teaches a parallel bus and wherein the tester further receives sampled data from the parallel bus (fig. 4, 7, col. 5, lines 67-68, col. 7, lines 53-68, Talley). 8. Claims 10, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,82981), Ooishi (US 6,396,76882) and Talley (US 5,301,156) as applied to claim 1,15 above, and further in view of Gunny (US 4,870,425). As per claim 10, Schneider, Ooishi and Talley substantially teach the claimed invention described in claim 1 (as rejected above). Talley also teaches that the comparing step further includes the step of obtaining a difference between the high-speed statistical signature and the expected signature (col. 7, lines 34-52, Talley). However Schneider, Ooishi and Talley do not explicitly teach the specific use of subtracting the signature from the expected signature.**

Gunny in an analogous art teaches that with each clock pulse, new data appears at the output of M1-7, and its signature is compared with that of the data out of M2-7 in subtractors D1:7 and D2-7 (fig. 7A, col. 19, lines 9-12, Gunny). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Gunny by including an additional step of subtracting the signature from the expected signature. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that subtracting the signature from the expected signature would provide the opportunity to indicate whether any data errors have occurred.

- **As per claim 24, Schneider, Ooishi, Talley and Gunny teach the additional limitations. Talley teaches the computer system obtaining a difference between the high-speed statistical signature and the expected signature (col. 7, lines 34-52, Talley). Gunny teaches subtracting the signature from the expected signature (fig. 7A, col. 19, lines 9-12, Gunny).**

9. Claims 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1), Ooishi (US 6,396,768 B2), Talley (US 5,301,156) and Gunny (US 4,870,425) as applied to claim 10 above, and further in view of Boles et al. (US 5,019,899).

As per claim 11, Schneider, Ooishi, Talley and Gunny substantially teach the claimed invention described in claim 10 (as rejected above). Talley also teaches statistical signature (col. 7, lines 45-52, Talley). However Schneider, Ooishi, Talley and Gunny do not explicitly teach the specific use of the method further comprising the step of: determining whether the circuit passes the test based upon the difference being less than a particular amount. Boles et al. in an analogous art teach that the bit difference accumulator. .. signature are achieved (col. 11, lines 13-25, Boles et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Boles et al. by including an additional step of using the method further comprising the step of: determining whether the circuit passes the test based upon the difference being less than a particular amount.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using of the method further comprising the step of: determining whether the circuit passes the test based upon the difference being less than a particular amount would provide the opportunity to provide a programmable threshold number to pass a circuit if the difference is less than a particular value.

- **As per claim 12, Schneider, Ooishi, Talley, Gunny and Boles et al. teach the additional limitations. Schneider teaches the method further comprising the step of: repeating the high-speed signature obtaining and comparing steps for at least one additional setting of the high-speed circuit (col. 7, lines 9-12, col. 8, lines 9-16, col. 8, lines 58-67, Schneider). Talley teaches statistical signature (col. 7, lines 45-52, Talley). Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) in view of Ooishi (US 6,396,768 B2), Talley (US 5,301,156) and Wong et al. (US 5,329,559).**

As per claim 13, Schneider teaches a method for testing a high-speed circuit having a first frequency of greater than one GHz, the method comprising the steps of: utilizing a tester to provide a signal to the high-speed phase and clock recovery circuit, the signal having a delay corresponding to a phase change, and reading an output signal from the high-speed phase and clock recovery circuit; repeating the utilizing and reading steps a particular number of times (fig. 5, col. 7, lines 9-12, col. 8, line 21 to col. 9, line 11, col. 11, lines 17-50, Schneider): and optionally repeating the high-speed statistical signature obtaining and comparing steps for at least one additional setting of the high-speed circuit (col. 7, lines 9-12, col. 8, lines 9-16, col. 8, lines 58-67, Schneider). However Schneider does not explicitly teach the specific use of a second delay.

Wong et al. in an analogous art teach a second sub-circuit that generates a second delayed data signal corresponding to said stored data signal after a predefined transition in said clock signal (col. 9, lines 64-67, Wong et al.). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Wong et al. by including an additional step of using a second delay.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a second delay would provide the opportunity to time synchronize the recovered clock and the data signal. Schneider also does not explicitly teach the specific use of comparing the high-speed statistical signature of the high-speed phase and clock recovery circuit to an

expected signature to determine whether the high-speed phase recover circuit operates as desired.

Talley in an analogous art teaches that signature generator 412 data errors have occurred (col. 7, lines 34-52, Talley). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Talley by including an additional step of comparing the high-speed statistical "signature of the high-speed phase and clock recovery circuit to an expected signature to determine whether the high-speed phase recover circuit operates as desired.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to produce a signature, which is statistically related to the correctness of a stream of data and verify the correct operation of the high speed circuit. Schneider also does not explicitly teach the specific use of the tester having a second frequency of not greater than one GHz.

However Ooishi in an analogous art teaches easy detection of a failure by the tester even if the tester applies external clock signal ext.ClK of a low frequency to the SORAM, and therefore the SDRAM can be tested by a more inexpensive tester (fig. 3, 52, 65, abstract, col. 42, lines 12-15, Ooishi). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Ooishi by including an additional step of using the tester having a second frequency of not greater than one GHz. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce cost of testing a high-speed circuit.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 81), Ooishi (US 6,396,768 82), Talley (US 5,301,156) and Wong et al. (US 5,329,559) as applied to claim 13 above, and further in view of Gunny (US 4,870,425). As per claim 14, Schneider, Ooishi, Talley and Wong et al. substantially teach the claimed invention described in claim 13 (as rejected above). Talley also teaches that the comparing step further includes the step of obtaining a difference between the high-speed statistical signature and the expected signature (col. 7, lines 34-52, Talley).

However Schneider, Ooishi, Talley and Wong et al. do not explicitly teach the specific use of subtracting the signature from the expected signature. Gunny in an analogous art teaches that with each clock pulse, new data appears at the output of M1-7, and its signature is compared with that of the data out of M2-7 in subtractors D1-7 and D2-7 (fig. 7A, col. 19, lines 9-12, Gunny).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Gunny by including an additional step of subtracting the signature from the expected signature.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that subtracting the signature from the expected signature would provide the opportunity to indicate whether any' data errors have occurred.

12. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829B1), Ooishi (US 6,396,76B82) and Talley (US 5,301,156) as applied to claim 15 above, and further in view of Wilson (US 5,212,601).

As per claim 22, Schneider, Ooishi and Talley substantially teach the claimed invention described in claim 15 (as rejected above). Schneider further teaches the system wherein the high-speed circuit is a high-speed phase and clock recovery circuit (col. 7, lines 9-12, Schneider) and reads at least one output signal from the high-speed phase and clock recovery circuit (col. 8, lines 48-57, Schneider). However Schneider, Ooishi and Talley do not explicitly teach the specific use of the system wherein the at least one signal has a delay corresponding to a phase change, wherein the tester further sweeps the delay to provide a plurality of delays.

Wilson in an analogous art teaches that the phase shifter produces a delay variable in precise increments over a wide range, causing a variable phase relationship between the time windows and the delayed data pulses (abstract, Wilson). Wilson also teaches that varying the delay ... phase-shift control means (col. 7, lines 41-53, Wilson). Wilson teaches that the phase shift means 43 comprises a multi-stage delay line 45 (fig. 4, 9b, col. 13, lines 23-24, Wilson). Wilson teaches that referring to FIGS. 10 and 11, the delay line 45... multiplexers 47 and 49 (col. 15, lines 34-39, Wilson).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Wilson by including an additional step of using the system wherein the at least one signal has a delay corresponding to a phase change, wherein the tester further sweeps the delay to provide a plurality of delays.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide information about the high-speed phase and clock recovery circuit using plurality of delayed signals.

Applicants respectfully traverse these rejections. For ease of review, claim 1 is reproduced below:

> **A method for testing a high-speed circuit having a first frequency of greater than one GHz, the high-speed circuit being a high-speed phase and clock recovery circuit, the method comprising:**
>
> **obtaining a high-speed statistical signature of the high-speed circuit using a tester having a second frequency of not greater than one GHz by oversampling an output of the high-speed circuit, the tester being external to the high-speed circuit; and**
>
> **comparing the high-speed statistical signature of the high-speed circuit to an expected signature.**

Claim 1

The Examiner has stated that Schneider does not explicitly teach the specific use of obtaining a high-speed statistical signature of a high-speed circuit using a tester having a second frequency of not greater than one GHz. Applicants agree.

The Examiner has thus cited Talley to make up the deficiencies of Schneider. However, Talley fails to teach or suggest obtaining a high-speed statistical signature of a high-speed circuit using a tester having a second frequency of not greater than one GHz by oversampling an output of the high-speed circuit, in cooperation with the other elements as recited in claim 1.

Talley's disclosure is limited to a signature generator, which is a parallel input polynomial signature analyzer that uses a series of linear feedback shift registers to produce a test signature and utilizing a signature generator to provide a polynomial signal analysis for a unique test signature (col. 7, lines 33-53). Talley fails to teach or suggest obtaining a high-speed statistical signature of a high-speed circuit by oversampling an output of the high-speed circuit, as recited in claim 1. Furthermore, Talley fails to teach or suggest oversampling any output within an integrated circuit or device to obtain a high-speed statistical signature.

Moreover, the combination of Schneider and Talley fails to teach or suggest obtaining a high-speed statistical signature of a high-speed circuit using a tester having a second frequency of not greater than one GHz by oversampling an output of the high-speed circuit, in cooperation with the other elements as recited in claim 1. The combination of Schneider and Talley merely provides a method for testing a high-speed circuit having a first frequency of greater than one GHz, the high-speed circuit being a high-speed phase and clock recovery circuit (according to the Examiner) and a signature generator, which is a parallel input polynomial signature analyzer that uses a series of linear feedback shift registers to produce a test signature and utilizing a signature generator to provide a polynomial signal analysis for a unique test signature. Applicants submit that the combination fails to teach or suggest obtaining a high-speed statistical signature of a high-speed circuit using a tester by oversampling an output of a high-speed circuit. As such, Talley fails to make up the deficiencies of Schneider. Thus, Schneider, in view of Talley, fails to teach or suggest claim 1.

The Examiner has also cited Ooishi as disclosing easy detection of a failure by the tester even if a tester applies an external clock signal ext.CLK of a low frequency to a SDRAM, and therefore the SDRAM can be tested by a more inexpensive tester; Wong has been cited as disclosing that data signals in a data recovery signal path must be delayed by the same amount of time as the signals, which go through a non-linear element used for clock recover; and Gunny has been cited as disclosing that with each clock pulse, new data appears at the output of M1-7, and its signature is compared with that of data from M2-7 in subtractors D1-7 and D2-7.

However, even in arguendo Oosihi, Wong, and Gunny provides the aforementioned disclosures, which Applicants do not concede, Ooishi, Wong, and Gunny all fail either singly or in combination with Schneider and Talley to obtain a high-speed statistical signature of a high-speed circuit using a tester having a second frequency of not greater than one GHz by oversampling an output of the high-speed circuit, in cooperation with the other elements recited in claim 1. Therefore, Schneider in view of Talley, Ooishi, Wong, and Gunny, fail to teach or suggest claim 1.

Applicant submits that claims 2-12 are also allowable since they depend directly or indirectly upon an allowable base claim.

Claim 13

Applicant submits that claim 13 is an independent claim that has similar limitations to that of independent claim 1. Accordingly, for at least the reasons mentioned above, claim 13 should be allowable over the cited references.

Applicant submits that claim 14 is also allowable since it depends directly or indirectly upon an allowable base claim.

Claim 15

Applicant submits that claim 15 is an independent claim that has similar limitations to that of independent claim 1. Accordingly, for at least the reasons mentioned above, claim 15 should be allowable over the cited references.

Applicant submits that claims 16-22 and 24 are also allowable since they depend directly or indirectly upon an allowable base claim.

Conclusion

In view of the foregoing, Applicants submit that claims 1-22 and 24 are in condition for allowance. Applicants respectfully request reconsideration and allowance of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

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Date

/Joseph A. Sawyer, Jr./
Joseph A. Sawyer, Jr.
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540